WRAP-AROUND GATE FIELD EFFECT TRANSISTOR

Abstract of the Disclosure:

Methods of forming field effect transistors having wrap-around, vertically-aligned, dual gate electrodes. Starting with a silicon-on-insulator (SOI) structure having a buried silicon island, a vertical reference edge is defined, by creating a cavity within the SOI structure, and used during two etch-back steps that can be reliably performed. The first etch-back removes a portion of an oxide layer for a first distance over which a gate conductor material is then applied. The second etch-back removes a portion of the gate conductor material for a second distance. The difference between the first and second distances defines the gate length of the eventual device. After stripping away the oxide layers, a vertical gate electrode is revealed that surrounds the buried silicon island on all four side surfaces.